## CLAIMS

What is claimed is:

1. A method for transferring data entries from a peripheral to a data queue in a host system memory, the method comprising:

determining a lower limit on a number of available data entry positions in the data queue; and

selectively transferring a current data entry to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value.

2. The method of claim 1, wherein the data entries are incoming data status entries, wherein the data queue is an incoming data status ring in the host system memory, wherein determining a lower limit on a number of available data entry positions comprises determining a lower limit on a number of available incoming data status entry positions in the incoming data status ring, and wherein selectively transferring the current data entry comprises selectively transferring a current incoming data status entry to the host system memory using a full cache line write if the lower limit is greater than or equal to the first value.

3. The method of claim 2, wherein the lower limit is determined at least in part according to a number of unused incoming data descriptors.

4. The method of claim 3, wherein the lower limit is determined at least in part according to a number of unused incoming data status entry positions remaining for a current incoming data descriptor.

5. The method of claim 4, wherein the lower limit is determined at least in part according to a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor.

6. The method of claim 5, wherein determining the lower limit comprises calculating a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor minus 1.

7. The method of claim 6, wherein the number of unused incoming data descriptors is the difference between an incoming data status pointer and an incoming data descriptor write pointer.

8. The method of claim 7, wherein the first value is a number of unused incoming data status entry positions remaining in a current cache line.

9. The method of claim 7, wherein the first value is a number of incoming data status entries per cache line.

10. The method of claim 3, wherein the first value is a number of unused incoming data status entries positions remaining in a current cache line.

11. The method of claim 3, wherein the first value is a number of incoming data status entries per cache line.

12. The method of claim 3, wherein the number of unused incoming data descriptors is the difference between an incoming data status pointer and an incoming data descriptor write pointer.

13. The method of claim 2, wherein the first value is a number of unused incoming data status entries positions remaining in a current cache line.

14. The method of claim 2, wherein the first value is a number of incoming data status entries per cache line.

15. The method of claim 2, further comprising selectively transferring the current incoming data status entry to the host system memory using a partial cache line write if the lower limit is less than the first value.

16. The method of claim 2, wherein selectively transferring the current incoming data status entry to the host system memory using a full cache line write comprises transferring the current incoming data status entry and any previous incoming data status entries for a current cache line to the host system memory using a full cache line write.

17. The method of claim 16, wherein the first value is a number of unused incoming data status entries positions remaining in the current cache line.

18. The method of claim 16, wherein the first value is a number of incoming data status entries per cache line.

19. The method of claim 16, wherein determining the lower limit comprises calculating the sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for a current incoming data descriptor minus 1.

20. A system for transferring incoming data status entries from a peripheral to a host system memory, comprising:

a descriptor management system in the peripheral, the descriptor management system adapted to determine a lower limit on a number of available incoming data status entry positions in an incoming data status ring in the host system memory, and to selectively transfer a current incoming data status entry to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value.

21. A peripheral system for providing an interface between a host computer and an external device or network, the peripheral system comprising:

a descriptor management system adapted to determine a lower limit on a number of available data entry positions in a data queue in a host system memory, and to selectively transfer a current data entry to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value.

22. The system of claim 21, wherein the data entries are incoming data status entries, wherein the data queue is an incoming data status ring in the host system memory, and wherein the descriptor management system is adapted to determine a lower limit on a number of available incoming data status entry positions in the incoming data status ring, and to selectively transfer a current incoming data status entry to the host system memory using a full cache line write if the lower limit is greater than or equal to the first value.

23. The system of claim 22, wherein the descriptor management system selectively transfers the current incoming data status entry to the host system memory using a partial cache line write if the lower limit is less than the first value.

24. The system of claim 22, wherein the descriptor management system determines the lower limit at least in part according to a number of unused incoming data descriptors.

25. The system of claim 24, wherein the descriptor management system determines the lower limit at least in part according to a number of unused incoming data status entry positions remaining for a current incoming data descriptor.

26. The system of claim 25, wherein the descriptor management system determines the lower limit at least in part according to a sum of the number of unused

incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor.

27. The system of claim 26, wherein the descriptor management system determines the lower limit as a sum of the number of unused incoming data descriptors and the number of unused incoming data status entry positions remaining for the current incoming data descriptor minus 1.

28. The system of claim 27, wherein the descriptor management system determines the number of unused incoming data descriptors as the difference between an incoming data status pointer and an incoming data descriptor write pointer.

29. The system of claim 22, wherein the first value is a number of unused incoming data status entry positions remaining in a current cache line.

30. The system of claim 22, wherein the first value is a number of incoming data status entries per cache line.

31. The system of claim 22, wherein the descriptor management system selectively transfers the current incoming data status entry and any previous incoming data status entries for a current cache line to the host system memory using a full cache line write if the lower limit is greater than or equal to a first value.

32. The system of claim 22, wherein the peripheral system is a network controller adapted to provide an interface between a host computer and a network.